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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/500,048	06/25/2004	Arild Wego	P16145-US1	9119

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EXAMINER	
RUTKOWSKI, JEFFREY M	
ART UNIT	PAPER NUMBER
2619	
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07/08/2008	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/500,048	WEGO ET AL.	
	Examiner	Art Unit	
	JEFFREY M. RUTKOWSKI	2619	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *07 April 2008*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *11-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *15 and 20* is/are allowed.

6)☒ Claim(s) *11-14 and 16-19* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *25 June 2004* is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *04/07/2008*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. **Claims 1-10** have been cancelled.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

4. **Claims 11-12, 14, 17-19** are rejected under 35 U.S.C. 103(a) as being unpatentable over McHarg et al. (US Pat 5,291,482), hereinafter referred to as McHarg in view of Acharya (US Pat 7,110,359).

5. For **claims 11 and 17**, McHarg teaches a high bandwidth packet switch **[title]**. The switch contains a time multiplexed write **210** and read **212** bus **[col. 5 lines 25-30 and figure 2]** (one or more time slot buses for transferring frames from a number of serial input/output lines located on a receiving side of the node to a number of serial output lines located. on the transmitting side of the node). A buffer is connected between the input and output ports. A

buffer manager uses pointers to allocate memory locations for storing packets **[abstract]** (one or two data buffers for each time slot bus at the receiving side of the node for buffering the frames from the input/output lines before transmission, said one or two data buffers being shared between all the input/output lines by means of respective pointers allocating one memory area in a data buffer for each of the input/output lines). A monitor circuit uses a timer to determine if a pointer is encountered within a certain time period **[col. 15 lines 30-33]** (a timer for each input/output line for indicating the time at which data transfer requests for the respective input/output line are to occur). Packet receivers **202** and transmitters **204** are connected to the time multiplexed write **210** and read **212** buses.

6. McHarg does not teach the First In First Out (FIFO) buffers for each serial line or the use of a scheduler. Acharya teaches the FIFO limitation absent from the teachings of McHarg by disclosing a multiport switch with a receiver and a transmitter which include a respective FIFO buffer **[col. 3 lines 60-63 and col. 7 lines 5-10]** (the serial input/output lines each having one respective FIFO into/from which bits corresponding to the associated serial line are shifted). Acharya teaches the scheduler limitation absent from the teachings of McHarg by disclosing the use of a scheduler **220 [figure 2]**. It would have been obvious to a person of ordinary skill in the art at the time of the invention to use FIFO buffers for each serial line in McHarg's invention to provide a level of burst protection. It also would have been obvious to a person of ordinary skill in the art at the time of the invention to use a scheduler in McHarg's invention to control access to memory.

7. For **claim 12 and 18**, the combination of McHarg and Acharya teach everything in **claims 11 and 17**. The teachings of McHarg in the rejection of **claims 11 and 17** discuss the

pointer being used for storing memory location information (wherein a pointer contains a data bus address of the first bite of the data area it is allocating).

8. For **claims 14 and 19**, the combination of McHarg and Acharya teach everything in parent **claims 11 and 17**. McHarg does not teach the use of a round-robin scheduling mechanism. Acharya teaches the round-robin scheduling limitation absent from the teachings of McHarg by disclosing a network device that uses weighted round-robin scheduling to service queues **[abstract]** (wherein the scheduler checks the input lines for data transfer requests by using a round-robin scheme on a transfer request register containing one entry for each input line indicating if a data transfer request for the respective input lines exists).

9. It would have been obvious to a person of ordinary skill in the art at the time of the invention to use a weighted round-robin scheduling mechanism in McHarg's invention to cure an overflow condition.

10. **Claim 13** is rejected under 35 U.S.C. 103(a) as being unpatentable over McHarg as modified by Acharya as applied to **claim 11** above, and further in view of Reid (US Pat 4,131,762).

11. For **claim 13**, the combination of McHarg and Acharya teach everything in parent **claim 11**. McHarg teaches a lookup table used by a router **208** maps logical destination to a physical packet channel number, which is then used to select a transmitter pointer FIFO **[col. 6 lines 22-27]** (wherein there is one connection table for each time slot bus at the receiving side, each entry in the connection table contains at least a data bus address pointing to a byte in the associated data buffer, the entries are arranged in the same order as their corresponding bytes are to be

transferred on the data bus). McHarg does not teach the use of a time-slot counter. Reid teaches the time-slot counter limitation absent from the teachings of McHarg by disclosing a time-slot counter is synchronized to a precision clock **[col. 7 lines 27-30 and figure 12]** (a counter, synchronized to a clock used by the time slot bus for transmission of timeslots, indicates which byte in the associated data buffer that presently is to be read out from the data bus buffer into a time slot in the associated data bus by indexing the entries of the connection table).

12. It would have been obvious to a person of ordinary skill in the art at the time of the invention to use a time-slot counter in McHarg's invention to generate memory addresses **[Reid, col. 7 lines 15-20]**.

13. **Claim 16** is rejected under 35 U.S.C. 103(a) as being unpatentable over McHarg as modified by Acharya applied to **claim 11** above, and further in view of Sanders et al. (US Pat 6,931,022), hereinafter referred to as Sanders.

14. For **claim 16**, the combination of McHarg and Acharya teach everything in parent **claim 11**. McHarg does not teach a minimum delay modus or a constant delay modus. Sanders teaches the dual operating modus absent from the teachings of McHarg by disclosing a time slot interchanger operates in a minimum delay mode or a constant delay mode **[col. 4 lines 38-44]** (wherein frames are transmitted through the time slot buses either in a minimum delay modus or in a constant delay modus; in case of minimum delay, bytes from an input line are transferred over a time slot bus in the same order as they arrived on the input line; and, in the case of constant delay, bytes in transfer on a time slot bus are identifiable and bytes from an input line

may be transferred over a time slot bus in an order different from the order they arrived on the input line).

15. It would have been obvious to a person of ordinary skill in the art at the time of the invention to use a dual operating modus (minimum delay or constant delay) in McHarg's invention to allow support for more than one transmission technique.

Response to Arguments

Argument for **claims 11 and 17**:

The claimed invention teaches one buffer between the input line and the TDM bus and one buffer between the TDM bus and the output line.

Response:

The claimed invention does not require two buffers. The claimed invention only requires a single buffer for a bus to be shared among all input lines. Figure 2 of McHarg discloses a single buffer that is assigned to a bus and is shared among all input lines.

Argument for **claims 11 and 17**:

In the claimed invention, the TDM bus is a centralized component (see Figure 1).

Response:

The Examiner is confused by the applicant's argument because the specification seems to suggest figure 1 is a conventional switch **[Specification, Background of the Invention lines 18-28]**.

Additionally, in regards to the applicant's arguments against the McHarg reference individually, one cannot show nonobviousness by attacking references individually where the

rejections are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.,* 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986). The combination of McHarg and Acharya disclose a centralized bus scheme as claimed in the current invention **[Acharya, figure 2]**.

Argument for **claims 11 and 17**:

The combination of McHarg and Acharya is technically improper because the combination is inoperable. In a packet switch as disclosed by McHarg, the packets are transferred to the buffer immediately upon arrival. Therefore, the addition of the scheduler from Acharya is meaningless and would not be considered by one of ordinary skill.

Response:

It is not clear how the combination is inoperable because both McHarg and Acharya deal with packet switched systems **[Acharya, col. 2 lines17-20; McHarg col. 1 lines 10-15]**.

The person of ordinary skill would seek out Acharya's scheduler because McHarg does not provide an adequate scheduling mechanism to move information from the transmitter buffer to the central buffer.

Argument for **claims 12-14, 16 and 18-19**:

The applicant asserts the Examiner has not responded to the arguments that were previously presented.

Response:

In the arguments for **claims 12, 14, 18 and 19** the applicant reiterated the arguments presented for **claims 11 and 17**. Therefore, the Examiner has already addressed the arguments.

In the arguments for **claims 13 and 16**, the applicant attack McHarg individually and does not address the other references in the combination.

1. Applicant's arguments filed 04/07/2008 have been fully considered but they are not persuasive, for the reasons stated above.

Terminal Disclaimer

2. The terminal disclaimer filed on 04/07/2008 disclaiming the terminal portion of any patent granted on this application which would extend beyond the expiration date of Application Number 10/526526 has been reviewed and is accepted. The terminal disclaimer has been recorded.

Allowable Subject Matter

3. **Claims 15 and 20** are allowed.

Conclusion

4. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to JEFFREY M. RUTKOWSKI whose telephone number is (571)270-1215. The examiner can normally be reached on Monday - Friday 7:30-5:00 PM EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Hassan Kizou can be reached on (571) 272-3088. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Jeffrey M Rutkowski
Patent Examiner
07/02/2008

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